CLAIMS

1. A method of determining a simultaneous switching output ("SSO") allowance for a digital switching device comprising:

calculating a first scaling factor from a first expected parameter value of a digital system and a first assumed parameter value used to generate a SSO guideline for the digital switching device.

2. The method of claim 1 further comprising steps of

multiplying the SSO guideline by the first scaling factor to obtain a product; and

taking the integer portion of the product to obtain a scaled SSO guideline.

3. The method of claim 1 further comprising steps of:

calculating a second scaling factor from a second expected parameter value of the digital system and a second assumed parameter value used to generate the SSO guideline; and

multiplying the first scaling factor and the second scaling factor to obtain the SSO allowance.

4. The method of claim 3 further comprising a step of

calculating a third scaling factor from a third expected parameter value of the digital system and at least a third assumed parameter value used to generate the SSO guideline, wherein the multiplying step further includes multiplying the third scaling factor with the first scaling factor and the second scaling factor to obtain the SSO allowance.

5. The method of claim 4 wherein the third scaling factor is calculated from the third assumed parameter value and from a fourth assumed parameter value used to generate the SSO guideline.

6. The method of claim 4 wherein the fourth assumed parameter value is one of the first assumed parameter value or the second assumed parameter value.

7. The method of claim 1 wherein the first assumed parameter value is selected from the group consisting of a printed wiring board inductance, a maximum ground bounce voltage, and a load capacitance.

8. The method of claim 4 wherein the step of calculating the first scaling factor comprises dividing an assumed printed wiring board inductance by an expected printed wiring board inductance,

the step of calculating the second scaling factor comprises dividing an expected maximum ground bounce voltage by an assumed maximum ground bounce voltage; and

the step of calculating the third scaling factor comprises dividing the assumed maximum ground bounce voltage by the assumed maximum ground bounce voltage added to a ground bounce voltage calculated from a difference between an expected load capacitance and an assumed load capacitance, the difference being multiplied by a voltage-per-capacitance.

9. The method of claim 1 further comprising steps of:

calculating a first maximum number of a first driver type for an I/O bank;

dividing a first actual number of the first driver type by the first maximum number to obtain a first I/O bank utilization;

calculating a second maximum number of a second driver type for the I/O bank;

dividing a second actual number of the second driver type by the second maximum number to obtain a second I/O bank utilization;

adding the first I/O bank utilization to the second I/O bank utilization to obtain a weighted average simultaneous switching output ("WASSO") for the I/O bank; and

comparing the WASSO against the SSO allowance.

10. The method of claim 9 further comprising steps of

calculating a third maximum number of a third driver type for the I/O bank; and

dividing a third actual number of the third driver type by the third maximum number to obtain a third I/O bank utilization, wherein the step of adding includes adding the third I/O bank utilization to the first I/O bank utilization and to the second I/O bank utilization to obtain the WASSO for the I/O bank.

11. The method of claim 9 further comprising steps of

calculating a third maximum number of a third driver type for an adjacent I/O bank;

dividing a third actual number of the third driver type by the third maximum number to obtain a first adjacent I/O bank utilization;

calculating a fourth maximum number of a fourth driver type for the adjacent I/O bank;

dividing a fourth actual number of the fourth driver type by the fourth maximum number to obtain a second adjacent I/O bank utilization;

adding the third I/O bank utilization to the fourth I/O bank utilization to obtain a second WASSO for the adjacent I/O bank;

adding the WASSO and the second WASSO to obtain a WASSO sum;

dividing the WASSO sum by two to obtain an average WASSO; and

comparing the average WASSO against the SSO allowance.

12. The method of claim 1, wherein the digital switching device has *N* I/O banks, *N* being an integer, further comprising steps of

calculating a weighted average simultaneous switching outputs ("WASSO") for each of the *N* I/O banks to obtain *N* WASSOs;

adding the N WASSOs to obtain a WASSO sum;

dividing the WASSO sum to obtain a device WASSO; and

comparing the device WASSO against the SSO allowance.

13. The method of claim 1 wherein the digital switching device is a field-programmable gate array ("FPGA").

14. The method of claim 9 wherein the first driver type is configurable.

15. A computer-readable medium having computer-executable instructions for performing the method of claim 1.

16. A digital switching system comprising:

a digital switching device having *N* I/O banks, where *N* is an integer, including a first I/O bank capable of driving a first maximum number of a first type of load and a second maximum number of a second type of load; and

receiving logic having a first number of inputs of the first type of load coupled to the first I/O bank and a second number of inputs of the second type of load coupled to the first I/O bank, wherein a first portion of a first I/O bank utilization is the first number divided by the first maximum number times 100%, a second portion of the first I/O bank utilization is the second number divided by the second maximum number times 100%, a first weighted average simultaneous switching output ("WASSO") of the first I/O bank being the first portion of the I/O bank utilization summed with the second portion of the I/O bank utilization, the first WASSO being less than 100%.

17. The digital switching system of claim 16 wherein the digital switching device is a field-programmable gate array ("FPGA") and the first I/O bank includes configurable drivers.

18. The digital switching system of claim 16 further comprising:

a second I/O bank adjacent to the first I/O bank capable of driving a third maximum number of a third type of load and a fourth maximum number of a fourth type of load; and

second receiving logic having a third number of the third type of load coupled to the second I/O bank and a fourth number of the fourth type of load coupled to the second I/O bank, wherein a first portion of the second I/O bank utilization is the third number divided by the third maximum number times 100%, a second portion of the second I/O bank utilization is the fourth number divided by the fourth maximum number times 100%, the first portion of the second I/O bank utilization being summed with the second portion of the second I/O bank utilization to obtain a second WASSO, the second WASSO being less than 100% and an average of the first WASSO and the second WASSO being less than a simultaneous switching output allowance.

19. The digital switching system of claim 18 where the third type of load is the same as the first type of load and the fourth type of load is the same as the second type of load.

20. The digital switching system of claim 16 wherein the *N* I/O banks are connected to receiving logic a plurality of loads having numbers and types of loads selected to provide *N* WASSOs for the *N* I/O banks wherein each of the *N* WASSOs is less than 100% and a sum of the *N* WASSOs is less than a simultaneous switching output allowance.

21. A system of evaluating a digital switching system for ground bounce voltage comprising:

means for calculating a simultaneous switching output ("SSO") allowance;

means for calculating a first weighted average simultaneous switching allowance ("WASSO") for a first I/O bank of a digital switching device in the digital switching system;

means for calculating a second WASSO for a second I/O bank of the digital switching device;

means for averaging the first WASSO and the second WASSO to obtain an averaged WASSO; and

means for determining whether to apply ground bounce voltage reduction techniques to the digital switching system.

22. In a computer system having a user interface including a display and a selection device, a method of entering data and viewing results from the display comprising:

generating a spread sheet having entry cells and at least one calculation cell on the display;

entering printed circuit board design parameters into a first set of entry fields;

entering specifications of receiving logic in a second set of entry fields;

entering physical descriptions of output loads in a third set of entry fields;

entering a number of drivers used and a maximum number of recommended drivers for a plurality of driver types in an input-output bank of a digital switching device; and

displaying a weighted average simultaneous switching utilization for the input-output bank in a first calculation cell.